SINGLE PHASE ASYMMETRICAL CASCADED MULTILEVEL INVERTER DESIGN FOR INDUCTION MOTOR

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Abstract— This paper presents a asymmetric cascaded 7 level multilevel inverter using fixed frequency level shifted carrier based pulse width modulation technique. This new control scheme is applied to 7-level asymmetric cascaded inverter design for induction motor load. Different firing angle control schemes in LSCPWM for 7- level asymmetric cascaded multilevel inverter are compared. In asymmetric cascaded MLI by using only 2-H bridges with 8 switches we can get 7 level output voltage where as in symmetric cascaded MLI 7 level output voltage is obtained by using 3- H bridges with 12 switches

Keywords— symmetric CMLI, asymmetric CMLI, level shifted PWM, THD, PD, APOD, POD, Single phase induction motor

I. INTRODUCTION

Multilevel Inverter (MLI) offers a number of advantages when compared to the conventional two-level inverter in terms of improved d.c. link utilization and harmonic spectrum. The stepped approximation of the sinusoidal output waveform with higher levels reduces the harmonic distortion of the output waveform and the stresses across the semiconductor devices and also allows higher voltage/current and power ratings. The reduced switching frequency of each individual switch of the inverter also reduces the switching losses and improves the efficiency of the inverter.

The different types of MLI are diode clamped, flying capacitor, cascaded MLI. Diode clamped requires more no of diodes and flying capacitor has capacitor balancing problem The cascaded H-bridge inverters having more no of advantages such as modular structure compare to other topologies such as modular structure and less no of components it is one of the topologies proposed for drive applications which meet the requirements such as high power rating with reduced THD and switching losses. The asymmetric MLI reduces the number of input DC sources required and increases the number of levels in the output. The modulation strategy used for reducing the THD is the level shifted carrier based PWM technique and the carriers used are the triangular waves with same amplitude and frequency. This device has the high power rating, less switching losses, less conduction loss and it has the ability to with stand high switching stresses in the series connection employed in this inverter design.. This method proves that the THD in the seven level output can be highly reduced by CLSPWM technique and most importantly the performance characteristics of the motor load can be improved by implementing the proposed idea.[1-4]

This paper is organized as follows: The topology of symmetric and asymmetric cascaded multilevel inverter is presented in Section II. The level shifted carrier PWM is presented in Section III. The study case implemented in matlab is presented in Section IV. The simulation results are presented in Section V .The conclusions are represented in Section VI..The references used are presented in Section VII

II. SYMMETRIC AND ASYMMETRIC CASCADED MULTILEVEL INVERTER TOPOLOGY

The topology of symmetric cascaded multilevel inverter is shown in Fig. 1. A seven -level symmetric cascaded H-bridge multilevel inverter has three H-bridges. The DC source for the three H-bridges H_1, H_2, H_3 is V_{dc}. In this topology the output voltage of the individual H bridges is $-V_{dc}$, 0 or $+V_{dc}$. Therefore the output voltage of the inverter can have the values $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$, which gives a five level output voltage. The switching states of symmetrical five level output voltage is given in the Table. 1. [5]

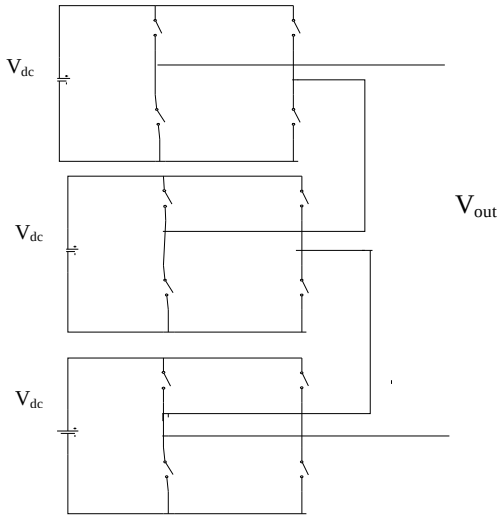

Fig. 1. Symmetrical cascaded seven level inverter Topology

The number of voltage levels (m) in the phase voltage of symmetrical CMLI inverter can be found from

$$m = (2N + 1)$$

Where N is the number of H-bridge cells per phase leg The maximum output phase voltage of these *N* cascaded multilevel inverters is

$$V_{0,\,MAX} = NV_{dc}$$

The total number of active switches used per phase in the CML inverters can be calculated by[6]

$$Nsw = 4N$$

Asymmetric multilevel have the same topology as symmetric multilevel inverters. They differ only in the rating of input dc voltages and control strategies. For many applications it is difficult to use separate dc sources and too many dc sources will require many long cables and could lead to voltage imbalance among the dc sources. To reduce the number of dc sources required for the cascaded H-bridge multilevel inverter, a scheme is proposed which uses lesser number of bridges. This scheme therefore provides the capability to produce higher voltages at higher speeds with low switching frequency which has inherent low switching losses and high converter efficiency. A seven-level asymmetric cascaded H-bridge multilevel inverter has two H-bridges for each phase. The DC source for the first H-bridge (H_1) is $V_{dc}/2$, while the DC source for the second bridge (H_2) is V_{dc}. The switching states of asymmetrical seven level output voltage is given in the Table. 1.

The number of voltage levels (m) in the phase voltage of symmetrical CMLI inverter can be found from

$$m = 2^{N+1}\text{-}1, \quad \text{if } V_{dc} = 2^{j-1}V_{dc}, \quad j = 1, 2, 3,\ldots N$$

Where N is the number of H-bridge cells per phase leg\
The maximum output phase voltage of these *N* cascaded multilevel inverters is

$$V_{0,\,MAX} = (2^{N+1}\text{-}1)V_{dc}$$

The total number of active switches used in the CML inverters can be calculated by

$$Nsw = 4N$$

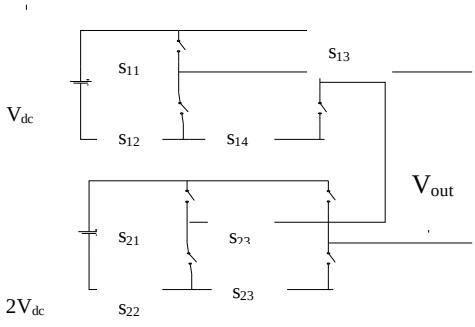

Fig. 2. Topology of asymmetrical cascaded seven level inverter

TABLE. 1.
SWITCHING PATTERN FOR SYMMETRIC CASCADED SEVEN LEVEL INVERTER

S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	S_{31}	S_{32}	S_{33}	S_{34}	o/p
0	1	0	1	0	1	0	1	1	0	0	1	V_{dc}
0	1	0	1	1	0	0	1	1	0	0	1	$2V_{dc}$
1	0	0	1	1	0	0	1	1	0	0	1	$3V_{dc}$
0	1	0	1	1	0	0	1	1	0	0	1	$2V_{dc}$
0	1	0	1	0	1	0	1	1	0	0	1	V_{dc}
0	1	0	1	0	1	0	1	0	1	0	1	0
0	1	0	1	0	1	0	1	0	1	1	0	$-V_{dc}$
1	0	0	1	0	1	1	0	0	1	1	0	$-2V_{dc}$
0	1	1	0	0	1	1	0	0	1	1	0	$-3V_{dc}$
1	0	0	1	0	1	1	0	0	1	1	0	$-2V_{dc}$
0	1	0	1	0	1	0	1	0	1	1	0	$-V_{dc}$
0	1	0	1	0	1	0	1	0	1	0	1	0

TABLE.2. SWITCHING PATTERN FOR ASYYMETRICAL CASCADED SEVEN LEVEL INVERTER

S_{11}	S_{14}	S_{13}	S_{12}	S_{21}	S_{24}	S_{23}	S_{22}	output
1	1	0	0	1	0	1	0	V_{dc}
0	1	0	1	1	1	0	0	$2V_{dc}$
1	1	0	0	1	1	0	0	$3V_{dc}$
0	1	0	1	1	1	0	0	$2V_{dc}$
1	1	0	0	1	0	1	0	V_{dc}
0	0	0	0	0	0	0	0	0
0	0	1	1	1	0	1	0	$-V_{dc}$
0	1	0	1	0	0	1	1	$-2Vdc$
0	0	1	1	0	0	1	1	$-3V_{dc}$
0	1	0	1	0	0	1	1	$-V_{dc}$
0	0	1	1	1	0	1	0	$-V_{dc}$
0	0	0	0	0	0	0	0	0

III. LEVEL SHIFTED PULSE WIDTH ODULATION TECHNIQUE

Modulation methods developed for multilevel inverters involve multilevel sinusoidal pulse width modulation. Multilevel selective harmonic elimination and space-vector modulation. It is generally accepted that the performance of any inverter, with any switching strategy can be related to the harmonic contents of its output voltage. There are many control techniques reported for cascaded multilevel inverter. But the popularly used modulation method is the multicarrier level shifted PWM technique. Level shifted PWM technique is the

generally used method in cascaded multilevel inverter as it gives a reduced THD. In this paper, fixed frequency PWM is proposed which uses the conventional sinusoidal reference signal and the carrier signals with variable frequency. To implement a m-level inverter, (m-1) carriers are used. There are six distinct carriers with fixed frequency and with the same magnitudes for the seven level multilevel inverter ; the difference between the carriers is that they are all displaced by a set of DC offset. The frequency modulation index is given by $m_f = f_c / f_m$

Where f_c = carrier frequency
f_m = modulating waveform frequency
Where as the amplitude modulation index is defined as
$ma = V_m/V_{cr}(m-1)$ for $0 \leq ma \leq 1$
Where V_m = peak value of the modulating waveform\
V_{cr} = peak value of the carrier waveform

the switching frequency of the inverter using the level-shifted modulation is equal to the carrier frequency, that is,

$$fsw,inv = fcr$$

and the average device switching frequency is

$$fsw,dev = fcr / 2N$$

The following figures shows the simulated waveforms for a seven-level inverter operating under the condition of $m_f = 57$, $m_a = 1.0$, $f_m = 50$ Hz, and $f_{cr} = 2850$ Hz. Although the carrier frequency of 2850 Hz seems high for high-power converters, the average device switching frequency is only 712 Hz.[6-11]

Figure 3,4 and 5 shows three schemes for the level-shifted multicarrier modulation:(a) in-phase disposition (IPD), where all carriers are in phase; (b) alternative phase opposite disposition (APOD), where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition (POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference.,

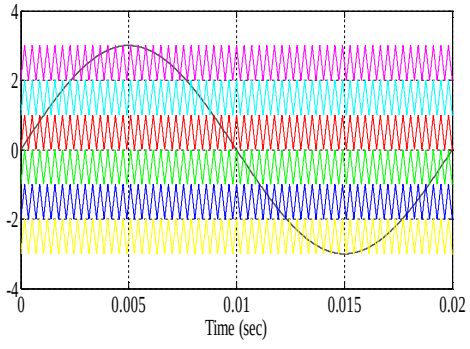

Fig.3.Reference and carrier waveform for PD CLSPWM

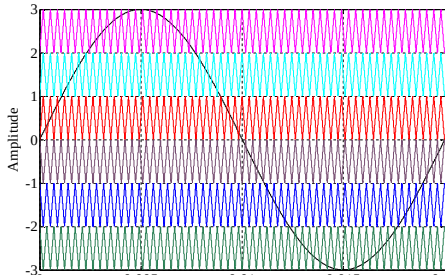

Fig.4.Reference and carrier waveform for POD CLSPWM

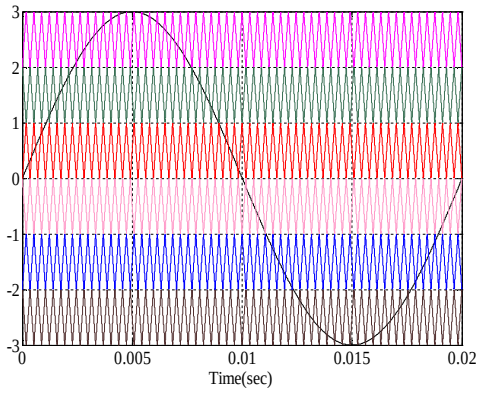

Fig. 5. Reference and carrier waveform for APOD CLSPWM

IV. STUDY CASE IMPLEMENTED IN MATLAB

The simulation of asymmetrical cascaded MLI is carried out using MATLAB/SIMULINK.it is shown in the fig.5.

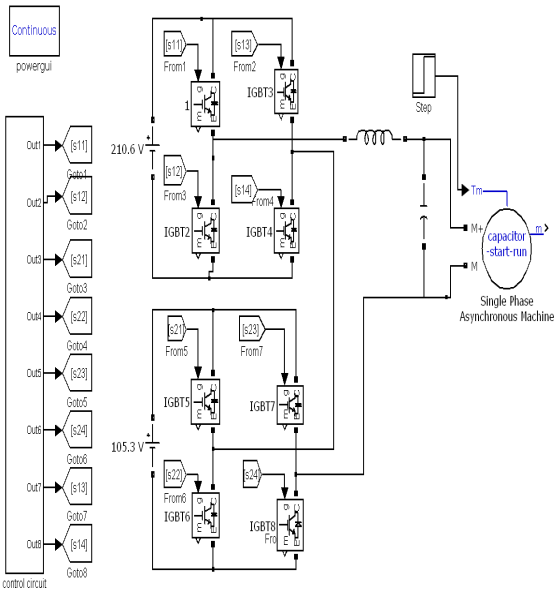

Fig.6. Simulation of asymmetrical seven level inverter

The control circuit of asymmetrical cascaded MLI is shown in the fig.6.

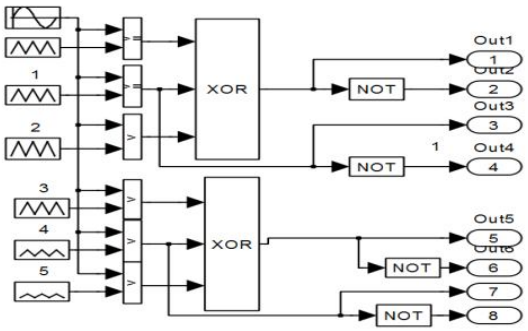

Fig. 7. Simulation control circuit of asymmetrical seven level inverter

V. SIMULATIONS RESULTS

The topology presented in this paper employs six carriers level shifted by particular amplitude. The performance analysis has been carried using a single phase induction motor and asymmetric inverter has been used for the analysis. The parameters of the motor are specified in Table 3

TABLE 3. INDUCTION MOTOR PARAMETERS

Parameters	Value
Voltage (V)	220
Frequency (Hz)	50
No. of pole pairs	2
Speed (rad/sec)	160

The output voltage waveform seven level asymmetric cascaded multilevel inverter with capacitor start-run induction motor load for 3 cycles using PD-CLSPWM is shown in Fig.8. and its FFT analysis is shown in Fig.9. The same voltage waveform using POD-CLSPWM is shown in Fig.10. and its FFT analysis is shown in Fig.11. And using APOD-CLSPWM is shown in Fig.12. and its FFT analysis is shown in Fig.13.

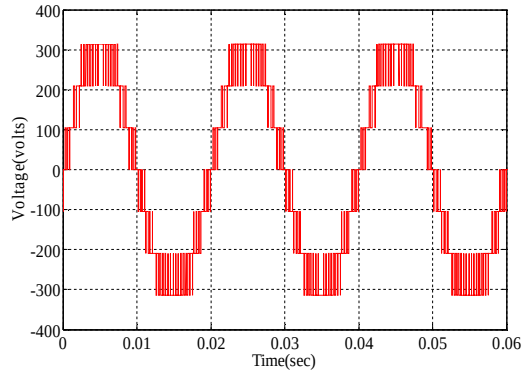

Fig. 8. Output phase voltage waveform for asymmetric (7-level) MLI using PD-CLSPWM

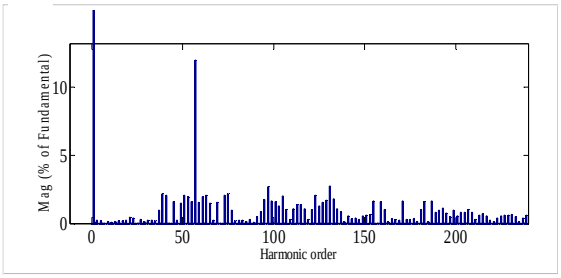

Fig. 9. FFT analysis of voltage waveform of asymmetric (7-level) cascaded multilevel inverter using PD-CLSPWM

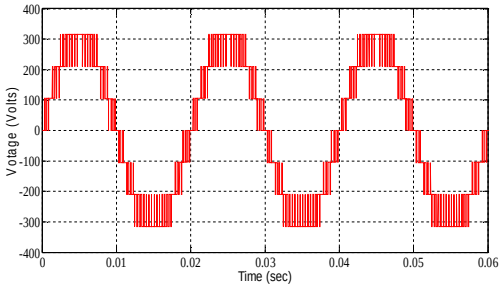

Fig. 10. Output phase voltage waveform for asymmetric (7-level) MLI using POD-CLSPWM

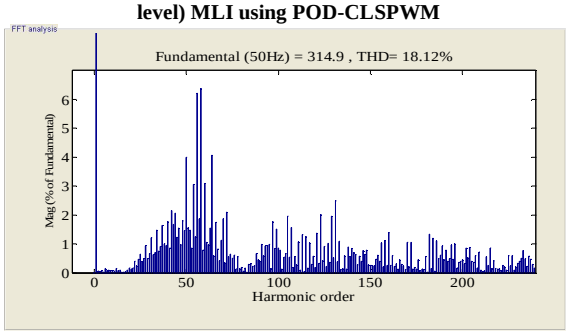

Fig. 11. FFT analysis of voltage waveform of asymmetric (7-level) cascaded multilevel inverter using APOD-CLSPWM

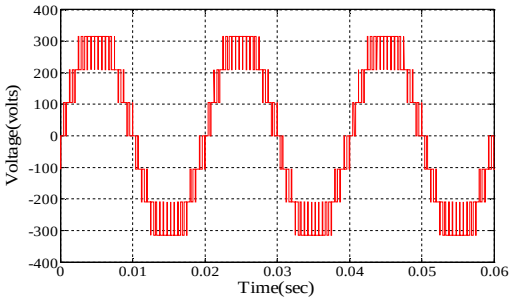

Fig.12.Output phase voltage waveform for asymmetric (7-level) MLI using POD-CLSPWM

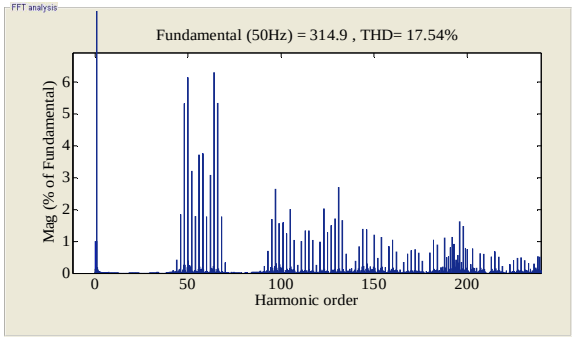

Fig.13.FFT analysis of voltage waveform of asymmetric (7-level) cascaded multilevel inverter APOD-CLSPWM

The analysis carried out for asymmetrical cascaded 7 level MLI using PD carriers PWM and single phase capacitor start-run induction motor as load. A LC filter is designed to reduce the THD of the output voltage to less than 5 %. The switching frequency of the inverter is f_s = 2850 Hz. The resonant frequency selected is 1000 Hz. The filter values are L=0.32mH and C = 0.32mF are selected. The output voltage with LC filter as shown in the fig.14. and its FFT analysis is shown in Fig.15.

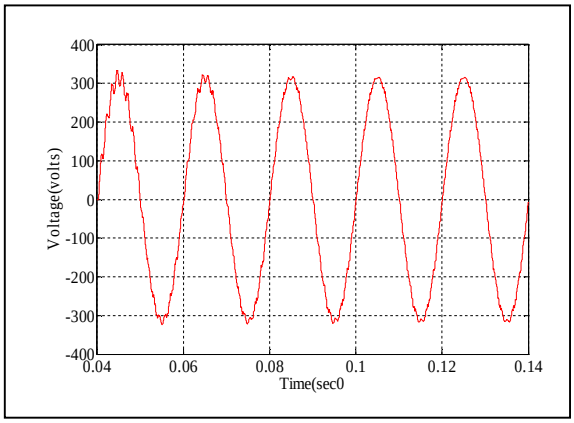

Fig.14.Output phase voltage waveform for asymmetric (7-level) MLI using PD-CLSPWM using LC filter

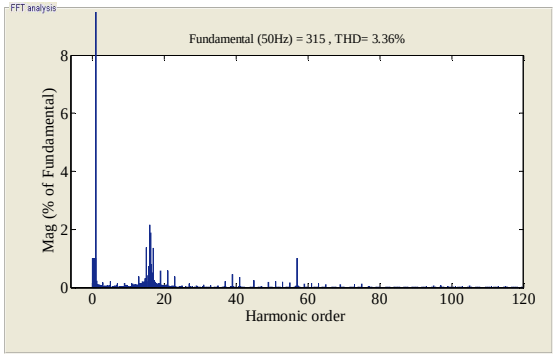

Fig.15.FFT analysis of voltage waveform of symmetric (7-level) cascaded multilevel inverter PD-CLSPWM using LC filter

With LC filter the all the higher order harmonics are eliminated and therefore the THD of the output voltage is reduced to 3.36%.The output current of the CMLI is shown in the fig.16. the other results of the single phase induction motor is shown in below figures

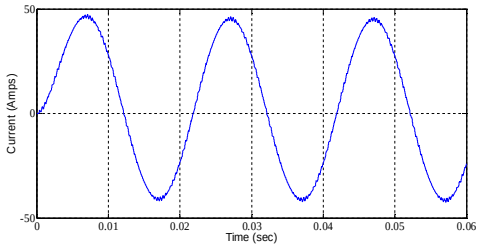

Fig.16. .output phase current waveform of asymmetric (7-level) cascaded multilevel inverter

The speed, main winding current and the torque of the induction motor are observed and are shown below

The speed, main winding current and Torque of the induction motor for 1 sec is shown in Fig.17. Fig.18., and Fig.19..

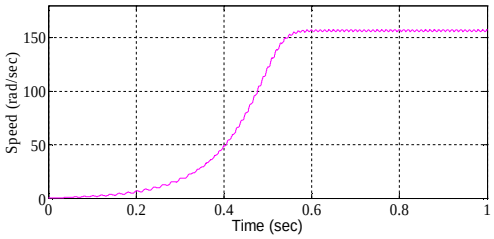

Fig.17.Speed of single phase induction motor

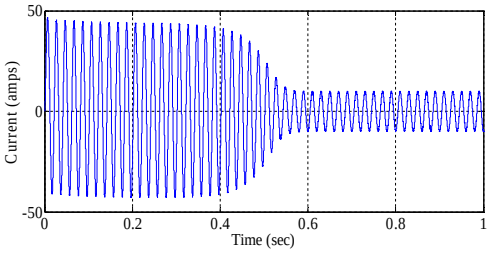

Fig.18.Main winding current of single phase induction motor

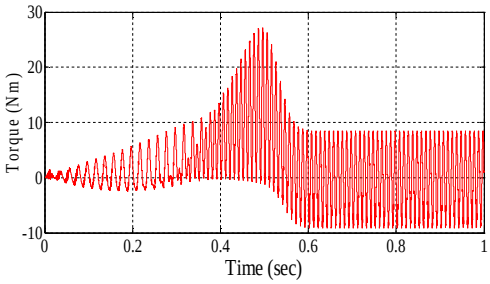

Fig.19.Torque of single phase induction motor

The THD of the output voltage of asymmetrical cascaded MLI is compared for the PD, POD, APOD techniques is shown in table.3

TABLE.3 THD (%) OF OUTPUT VOLTAGE

	PD	POD	APOD
Voltage THD(%)	18.01	18.12	17.54

CONCLUSIONS

In asymmetrical topology the output voltage is seven level by using only 2 bridges (8 switches) where as symmetrical topology uses 3 bridges(12 switches).therefore the number of switches are reduced in asymmetrical topology compared to Symmetrical topology for the same no of levels. The THD of the voltage of asymmetrical CMLI is studied under different modulation techniques such as PD,

APOD, POD and the less THD is observed for APOD technique

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