COMPARISON STUDY OF 1-BIT FULL ADDER DESIGN USING DIFFERENT TECHNOLOGIES

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Abstract—The adder is an important unit in any processor and controller circuit. There are so many full adder circuits which have been proposed and designed. In this proposed work a 1-bit hybrid full adder circuit using Complementary Pass Transistor Logic and Transmission Gate Logic is designed and then compared with the existing designs such as C-CMOS, CPL, 24-T full adder, TGL, Transmission Function Adder and hybrid full adder using C-CMOS and TGL logic designs. Comparative descriptions of various parameters like propagation delay, power consumption and Power Delay Product have been done.

The result shows that delay is reduced by 68.037%, average power reduced by 18.90% and PDP is reduced by 12.84%.

Keywords—XOR gate, Transmission Function Adder, Complementary CMOS.

I. INTRODUCTION

Addition is the basic arithmetic operation and is used in VLSI system as a full adder circuit extensively. It adds binary numbers and is the main part for other operations such as subtraction (complement addition), multiplication (successive addition) and division (successive subtraction) etc. The overall performance of system is mainly dependent on adder performance.

Hence performance enhancement is addressed at different design levels such as the architectural circuit, layout and process technology level. At circuit design level power savings exists by means of proper choice of a logic style for implementing combinational circuit. This is because all the important parameters governing the power dissipation- switching capacitance, transition activity, and short circuit currents-are strongly influenced by choose logic design style.

II. EXISTING FULL ADDER DESIGNS

There are various new designs proposed regarding optimization of low power, high speed full adders by trying different options for logic styles like standard CMOS, CPL, 24T full adder, TGL, TFA and hybrid full adder using C-CMOS and TGL.

Standard CMOS full adder:The conventional CMOS full adder cell using 28 transistors based on standard CMOS topology has been discussed. It is described in that due to high number of transistors its power consumption was high and also the large PMOS transistors in pull up network resulted in high input capacitances which cause high delay and dynamic power.

Complementary Pass Transistor Logic full adder:CPL uses only an NMOS network for the implementation of logic functions, this result in low input capacitance and high speed operation. Because the high voltage level of the pass transistor output is lower than the supply voltage level by the threshold voltage of the pass transistors, the signal have to be amplified by using CMOS inverter at the output. The advantages of pass logic transistors include smaller number of transistors. The disadvantage of pass transistor logic is that threshold voltage drop through the NMOS transistors make it necessary to maintain output voltage level.

Fig 2.1: Circuit diagram of standard full adder

Fig 2.2: Circuit diagram of CPL full adder
24 T full adders: The 24 T full adder is based on bridge style. It has 24 transistors. It have better power consumption but the sum generator should wait to receive the Cout signal from the Cout generator: therefore the delay of 24 T FA is high.

Transmission Gate Logic full adder: A transmission gate is defined as an electronic element that will selectively block or pass a signal level from input to output. It consist two MOSFETs one N-channel responsible for correct transmission of logic zero and one P-channel is responsible for correct transmission of logic one. So transmission gates are widely used as CMOS design style to implement digital function. Transmission gate based implementation is similar to pass transistor with the difference that the transmission gate logic uses both the NMOS and PMOS transistors connected in parallel whereas pass transistor logic uses only one type of transistor i.e. either NMOS or PMOS. Full adder implementation based on TG logic uses 20 transistors.

1-bit hybrid full adder using C-CMOS and TGL: XNOR module is responsible for most of the power consumption of the entire adder circuit. Therefore this module is designed to minimize the power to the best possible extend by deliberate use of weak inverter 9channel width of transistor being small) formed by transistor M_p1 and M_n1. Full swing of output signal level is guaranteed by level restoring of transistor M_p3 and M_n3. The modified XNOR represented in this design offers low power and high speed compared with other XOR/XNOR circuits. While the output carry signal is implemented by transistor M_p7 M_p8, M_n7 and M_n8. The input carry signal is propagates only through a single transmission gate (M_p7 and M_n7) reducing the overall carry propagation path significantly. The deliberate use of strong transmission gate (channel width is made high) guaranteed further reduction in propagation delay of carry signal.
other so we will use CPL and TGL to make hybrid design. CPL is complementary pass transistor logic and TGL is transmission gate logic. CPL have small carry propagation path so small delay, good voltage swing restoration but there are few problems with CPL techniques that it can be used only for high power application and gives high voltage degradation. This voltage degradation can be overcome by the TGL but still some disadvantages like slow speed and high power consumption remain an area of concern so a new technique is applied called hybrid.

So we are proposing a modified circuit with better performance parameters that it reduced delay to 213.78ps and power to 4.54uW for 180nm technology at 1.8volt power supply. For 32 bit RCA circuit the delay is of 765ps and average power consumption is of 0.17uW. In fig. 2.8 1-bit hybrid full adder circuit is represented in which three inputs as A, B and cin is given and two outputs are taken as sum and cout.

### III. SIMULATION METHODOLOGIES

#### 3.1 Performance Parameters: Parameters of concern for backend are delay, PDP, power dissipation, area we need a design a circuit that is cost efficient and have better performance parameters then in base paper. Different logic styles tend to trade off with the performance of other.

#### 3.2 Backend: The tanner EDA Tool has been used so after the verification of a circuit on frontend we move on to backend with tanner EDA although there are many other costly tools available in market we will draw the schematic of modules for full adder that is provided in the base paper in S-edit using the software and initially we will divide the entire circuit into modules to elude further complications into results. Once we are done with S-edit the we will switch to W-edit automatically for the waveform generation to verify the circuit for each module we will compile the modules into a circuit and then than Now the step is fabrication that is not done in India as it cost to high. Tanner tool schematic for hybrid 1-bit full adder with C-CMOS and TGL is given as-

As full adder circuit is proposed by using CPL and TGL. Tanner tool schematic for hybrid 1-bit full adder is given as-
Performance parameters analysis
Delay improvement of 11.16% for modified 1 bit full adder as compared to best design for hybrid full adder [3] and average power consumption reduction to 34.63%. As a ground always waste the power, A 32-bit carry propagation adder is implemented as an extension of the proposed 1-bit full adder. It is a non-carry look-ahead adder structure where the carry propagation takes place every time till the last adder block. Performance parameters can be calculated by varying the width of each transistor one by one final width are seated and a table is formed to where every transistor is defined with the optimized width and length to get the most satisfactory results compared to existing design technologies.

Table 4.1: Simulation result for full adder in 180 nm technologies at 1.8V.

<table>
<thead>
<tr>
<th>Technologies</th>
<th>Delay (ps)</th>
<th>Average Power(μW)</th>
<th>PDP (fJ)</th>
<th>Transistor</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>TGL</td>
<td>293.9</td>
<td>8.4719</td>
<td>2.8989</td>
<td>20</td>
<td>[9]</td>
</tr>
<tr>
<td>24 TF A</td>
<td>151.2</td>
<td>15.91</td>
<td>4.998</td>
<td>24</td>
<td>[10]</td>
</tr>
<tr>
<td>TFA</td>
<td>287.1</td>
<td>8.2491</td>
<td>2.3683</td>
<td>16</td>
<td>[11]</td>
</tr>
<tr>
<td>Hybrid full adder</td>
<td>241.25</td>
<td>4.6</td>
<td>0.931</td>
<td>16</td>
<td>[3]</td>
</tr>
<tr>
<td>32 bit RCA modified</td>
<td>765.33</td>
<td>0.17</td>
<td>0.13</td>
<td>448</td>
<td>proposed</td>
</tr>
<tr>
<td>Modified full adder 180nm</td>
<td>213.78</td>
<td>3.007</td>
<td>0.642</td>
<td>14</td>
<td>proposed</td>
</tr>
</tbody>
</table>

CONCLUSION
In this paper, various designs of full adders have studied at various design technologies. A high speed hybrid full adder is designed to overcome the problems of other designs for full adders and for fast execution of system we require an adder with less power dissipation. A low-power high speed modified hybrid 1-bit full adder has been proposed the design has been extended for 32-bit ripple carry adder also. The proposed full adder offered 24.14% improvement with respect to the best reported design [25] in terms of PDP (180-nm technology at 1.8 V). The proposed full adder was further used to implement a 32-bit ripple carry propagation adder at 180nm technology at 1.8V.

REFERENCES
Comparison Study of 1-Bit Full Adder Design Using Different Technologies


