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STEADY STATE AND FAULT ANALYSIS IN HVDC TRANSMISSION NETWORK BASED ON HYBRID CASCADED MULTILEVEL VSC

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Abstract- The evolution of high-voltage fully controlled semiconductor technology has significant impact on efficient management of electrical grids. This paper proposes a high-voltage DC (HVDC) transmission systems based on a hybrid multilevel voltage source converter (VSC) with ac-side cascaded H-bridge cells. It deals with the control of Multilevel VSC-HVDC, the use of VSC-HVDC in a large network consisting of a bipolar transmission system. The objective of the work is to assess the performance of a VSC-HVDC with ac-side cascaded H-bridge cells during DC pole to pole fault. A control system is developed combining an inner modulator and capacitor voltage balancing controller, an intermediate current controller and an outer active and reactive power controller. The control strategy based on PI and Fuzzy are studied and simulated in MATLAB / SIMULINK.

Keywords- Cascaded H-Bridge, Fuzzy, PI Controller, VSC-HVDC

I. INTRODUCTION

The HVDC technology is a high power electronics technology used in electric power systems. It is an efficient and flexible method to transmit large amounts of electric power over long distances by overhead transmission lines or underground/ submarine cables. It can also be used to interconnect asynchronous power systems.

Recently a new type of HVDC has become available. It makes use of the more advanced semiconductor technology instead of thyristors for power conversion between AC and DC. The semiconductors used are insulated gate bipolar transistors (IGBTs), and the converters are voltage source converters (VSCs) which operate with high switching frequencies (1-2kHz) utilizing pulse width modulation (PWM)[2].

The VSC-HVDC technology has a higher control capability when compared with the classic alternative, since it can independently control the active and the reactive power exchanged with the connected AC network.

Additionally, the footprint of a VSC station is smaller, since the filters needed are smaller – due to the use of PWM techniques - and this is a key factor, since building large structures offshore tends to be expensive. Furthermore, with VSCs there is no need for reactive power compensation and the necessary communication between stations is smaller making this technology more attractive for offshore purposes.

The AC-side voltage waveform of a multi-module VSC system is a multi-level wave-form with low harmonic distortion content provided that an appropriate harmonic cancellation/ minimization technique is used. Harmonic cancellation/minimization for a multi-module VSC system is conventionally achieved based on the phase-shifted carrier SPWM techniques. The main feature of this strategy is its simplicity for implementation.

However the use of carrier based level shifted PWM method is most suitable for a multilevel converter.

The H Bridge cells which are used along with the two level converters will eliminates the harmonics and thereby use of filters can be avoided. A combination of fuzzy and Pi controller implementation helps to provide a smooth and efficient control of VSC .The requirement of the highly rated circuit breakers can be avoided by using a hybrid cascaded multilevel topology in VSC.

II. OPERATIONAL PRINCIPLE AND CONTROL OF HYBRID MULTILEVEL VSC

A. Proposed Converter Topology

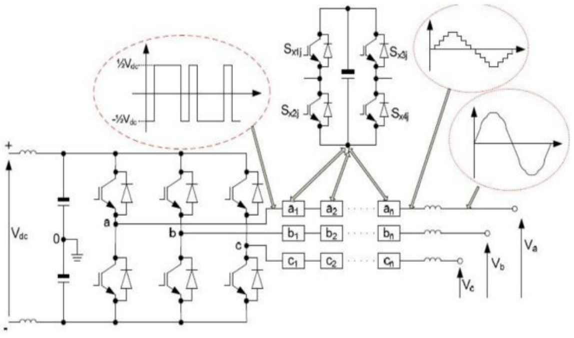


Fig 2: Hybrid multilevel converter with ac side cascaded H-Bridge cells.

The fig 2 shows the schematic diagram of a hybrid multilevel VSC with N H-bridge cells per phase. The series H-bridge cell uses low voltage rated gate commutated switching devices such as IGBTs with a maximum voltage stress limited to cell capacitor voltage. The circuit requires robust capacitor voltage balancing to ensure that voltage across each cell capacitor will not exceed the switch device rating under any condition. Each converter can generate 4N+1 voltage levels at converter terminal "a" relative to supply midpoint "o". Thus, as the number of cells per phase increases, the converter presents near pure sinusoidal voltage waveform.

The two level converter terminals will operates at 150-Hz switching frequency, therefore small audible noise along with switching losses are expected. As a solution to avoid this H-bridge cells are used in between "a" and point of common coupling (PCC).The H-bridge cells act as a series active harmonic filter to attenuate the low order harmonics in the output phase voltage, thereby creating a multilevel converter terminal voltage waveform with voltage steps equal to the cell capacitor voltage. Thus the winding voltage stress of the interfacing transformer (low dv/dt) decreases. The most important feature of this topology is the low switching losses due to the usage of low switching frequency for the two level converters as well as for the H-bridge cells. The level shifted carrier based multilevel PWM with 1-kHz switching frequency is used to control H-bridge cells. The sum of voltage across the H-bridge capacitors should be maintained Vdc/2, so as to minimize the conversion losses in the H-bridge.

III. PERFORMANCE EVALUATION & SIMULATED RESULTS

In order to evaluate the Hybrid multilevel converter with ac side cascaded H-bridge cells, the system is simulated in Matlab-Simulink.

a) Steady state analysis

The first case evaluates the steady state performance and active power reversal in the HVDC link.

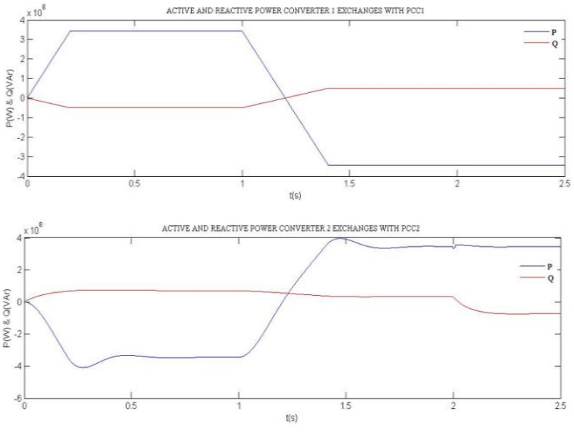


Fig 2.1: real and reactive power at PCC_1 and PCC_2

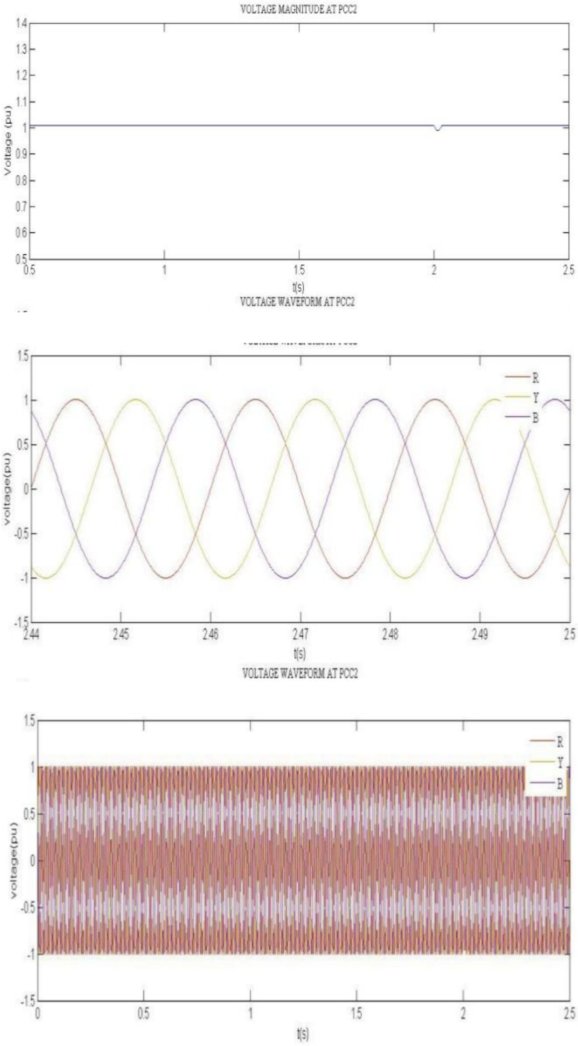


Fig 2.2: voltage magnitude and voltage waveforms at PCC_2

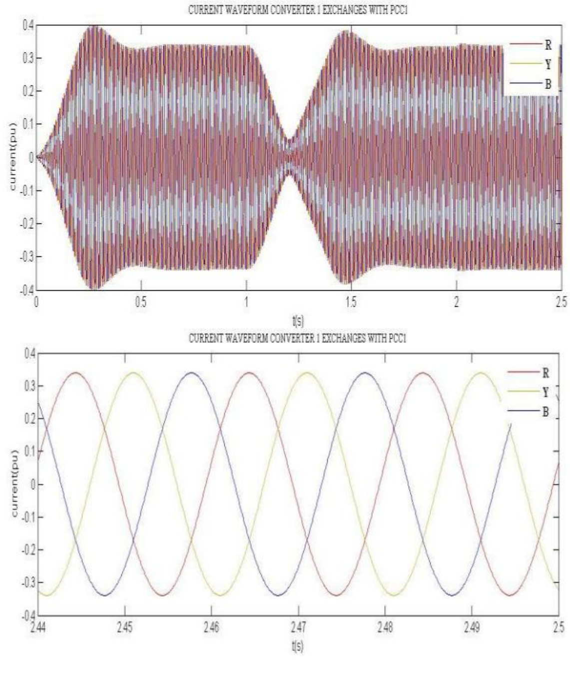


Fig 2.3: Current waveform that converter 1 exchanges with PCC_1

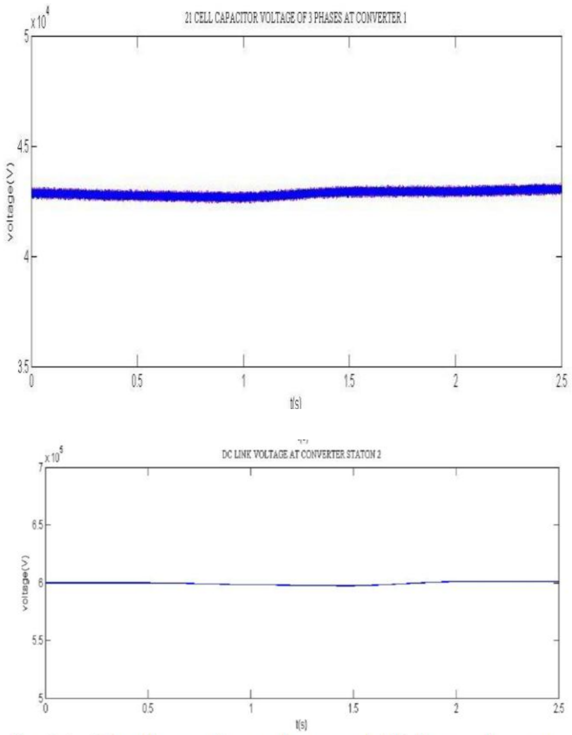


Fig 2.4: 21 cell capacitor voltage and DC line voltage at converter station 1 and 2 respectively

The fig 2.1 shows the key waveforms when the system exported 343.5 MW from G1 to G2. At t=1s, the power flow is reversed in order to import 343.5 MW to G1 from G2. In order to illustrate the voltage support capability of the Converter station 2, a load of 120+j90 MVA is introduced at t=2s to PCC2. During the entire operating period, the PCC1 and PCC2 reactive power are exchanged in order to support voltage. The fig 2.1 shows the active and reactive power exchange of converter 1 and converter 2 with PCC1 and PCC2 respectively. The fig 2.2 shows that converter 2 adjust its power exchange with PCC2 to maintain its voltage magnitude as there is a load is introduced at t=2s. The results shown in fig 2.2 and 2.3 proves that without use of any ac filters the converter 2 injects and provide high quality current and voltage waveforms at PCC2. The waveform shown in fig 2.4 demonstrates that the total 21 cell capacitor voltage of the converter 2 is maintained at desired set point during the entire operating period. Also the total DC link voltage is regulated at 600kV as shown in figure 2.4.

b) DC fault analysis

In order to analyze the performance of H- Bridge VSC during a dc fault, pole to pole fault is applied to the network in the period between 1 and 1.4 seconds. As a result the active power exchanges between the two grids is falls to zero and also the converter switches inhibits the flow of power through the converter to eliminate the grid contribution. Fig 3.1 shows active and reactive power converter 1 and 2 exchanges with PCC1 and PCC2. respectively. In order to restart the system after the fault, converters gating signals are to be activated and power surges are also introduced as shown in fig 3.2.

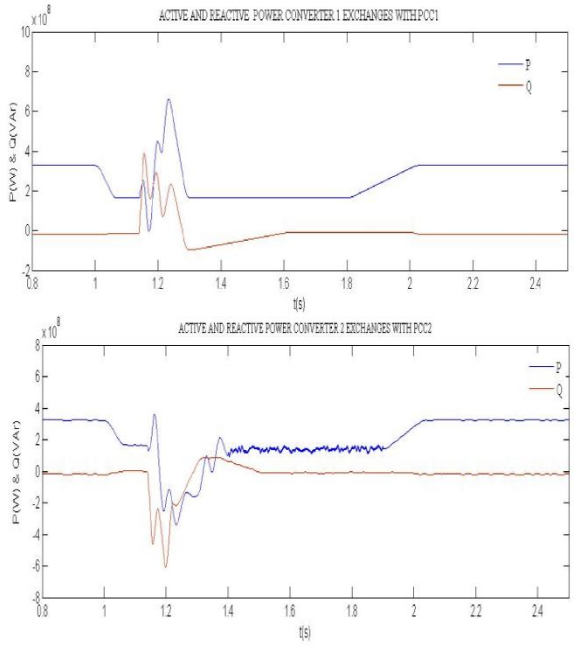


Fig 3.1 Real and Reactive power that converters exchanges to PCC1 and PCC2 respectively.

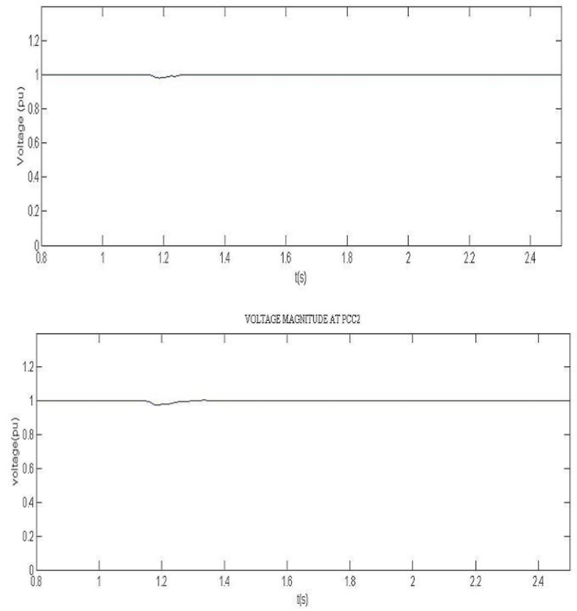
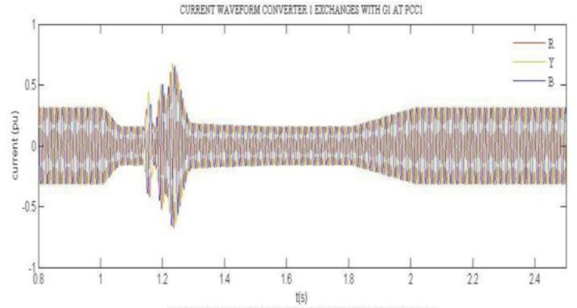


Fig 3.2 voltage magnitude at PCC_1 and PCC_2



CURRENT WAVEFORMS CONVERTER 2 EXCHANGES WITH GRID G2 AT PCC2

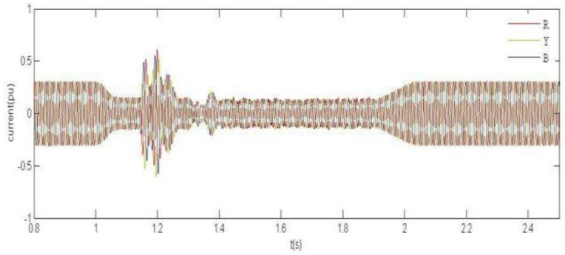


Fig 3.3 Current waveforms converter 1 and 2 exchanges with grid G_1 and G_2 respectively.

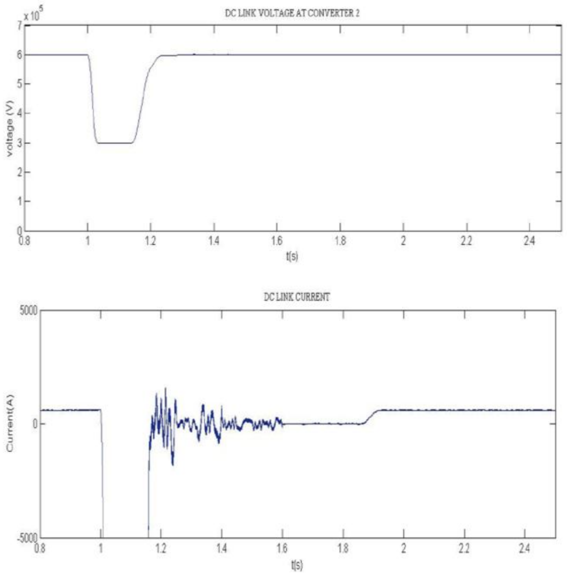
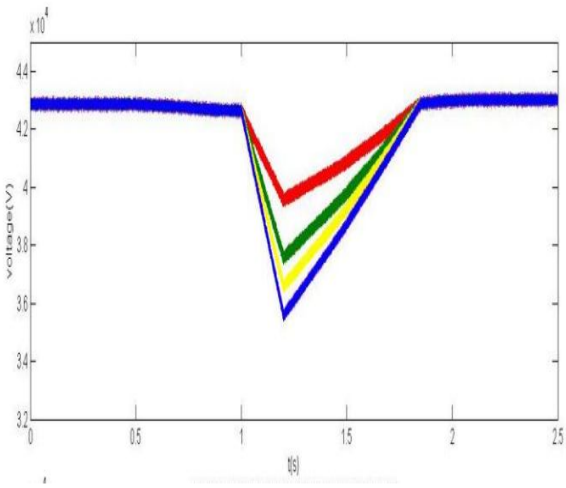


Fig 3.4 DC link voltage and current waveforms

From the fig 3.2 it is found that there is a dip in magnitude of voltage at both PCC1 and PCC2 due to the sudden consumption of reactive power for the start-up of the system after fault. There will be current surges at both converter station sides since the dc side capacitors try to charge from the ac sides of the system during fault period as shown in fig 3.3.



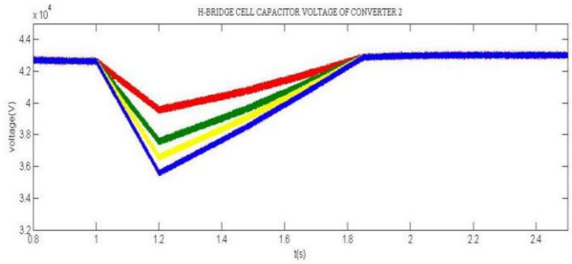


Fig 3.5 H-bridge cell capacitor voltage of converter 1 and 2

The fig 3.4 shows that the converter 2 is capable to come to its actual state after the fault is cleared however the time taken to recover is quite large. After the fault clearance, the ac grid will act along with dc link current to charge the capacitors across dc link. As shown in fig 3.5, it is found that dc link capacitor voltage across both converters will also reduced during fault in order to regulate the active power. By using cell capacitors of high capacitance, the reduction in capacitor voltage can be minimized.

CONCLUSION

This paper investigates a fault resilient VSC technology for high voltage transmission system with better power control capability during DC grid fault. The main advantage of this system is its fault blocking ability without reducing the active power exchange between the ac networks to zero during a dc fault period. As the magnitude and duration of dc fault current is less, this technique also simplifies the dc circuit breaker design.

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