DESIGN AND ANALYSIS OF FINFET BASED HIGH PERFORMANCE 1-BIT HALF ADDER-HALF SUBTRACTOR CELL

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Abstract- we are moving towards the era of minimization of transistor size, short channel effects (SCEs) are becoming major concern. Double gate FinFETs are emerging transistors, which gives better SCEs performance compared to conventional Mosfet transistors .Adders and sub-tractors are very basic components in computation. Most of the operations such as multiplication, division, ripple carry addition etc. require Adder and sub-tractor as a basic building block. The efficiency of any system depends on the performance of internal components. If internal components satisfy the criteria of area, power and delay, the system will always be a efficient system. The adders and sub-tractors are mainly used in (arithmetic and logical units) ALUs. In this paper, area and (power delay product) PDP efficient common Half Adder-Half sub-tractor cell design is presented at 32nm technology.

Keywords- Alu; Double Gate Finfet (Dgfinfet); Delay; Half Adder; Half Subtractor; High Performance; Low Power.

I. INTRODUCTION

In today's trend, any portable electronic devices like mobiles, Laptops, iphones etc. should be smarter and smaller. Smarter device means, it should respond fast and smaller device context in terms of cost and area. To meet these specifications, We should proceed from system to circuit level. Every processor has one arithmetic logic unit (ALU) inside it. Addition and subtraction are the two basic operations performed by ALU. There are two separate cells for Addition and subtraction operations. If one common cell is able to perform both the operations then area on chip can be reduced by approximately half. This is the main idea behind this paper.

As the CMOS process moving towards short channel length, then channel resistance gets reduce and delay offered by the transistor can be reduces. But minimum channel length introduces Short channel effects (SCEs). In short channel devices flow of the current is not only controlled by gate electrode but also drain supply. As drain voltage decreases barrier between source and drain. This is called as "Drain induced Barrier Lowering" (DIBL). With single gate, It is very hard to control current flow in OFF mode of transistor and there will be always OFF current (Ioff). Hence, it is not possible to completely off the Transistor. SCEs limit the further reduction in channel length. In short channel devices threshold voltage is decreased but results in exponential increment in sub threshold leakage current [4]. Due to SCEs, sub-threshold leakage power consumption increases in short channel devices. Power Consumption is also a main concern in portable devices. Silicon On-insulator (SOI) technology gives better results than bulk Technology. SOI helps to improve circuit performance, high reliability and removes the parasitic capacitances and punch through issues [3]. Based on SOI technology a novel Double gate fin- type field effect transistor introduced, named as DGFinFET. Figure1 shows the cross-sectional view of DGFinFET transistor. Since channel will forms on Buried oxide (BOX), which helps to reduces junction leakage current and junction capacitances. DGFinFET is 3D device which have two gates, both sides of fin. For short channel length, two gates, on both sides of the Fin provides a good control on the channel compared to single gate device (MOSFET). This allows very small off current to flow and use of less threshold voltage (Vth) [1].

GFinFET offers improved SCE effects compared to MOSFET. As per the Application DGFinFET can be used as Shorted Gate (SG) and Independent Gate (IG), from figure (2). In SG mode, both gates are shorted together and gates can be configuring at different potential in IG mode [3]. The effective channel width of multi gate device is given by following [10].

$$Weff \sim 2Hfin + Tfin \qquad (1)$$

Where Tfin is thickness of the Fin and Hfin is Height of the fin. Increase in effective width of the device increases the current and load capacitance in the same ratio, therefore delay gets affected [3]. Hence, channel width is restricted by Height of the Fin (Hfin). In any circuit, equal rise and fall time can be achieved by proper sizing of the transistors. Sizing in DGFinFET based circuits done by increasing number of fins. In this paper, 1-bit Half Adder-Half sub tractor cell is implementing with the help of shorted gate (SG) DGFinFET.

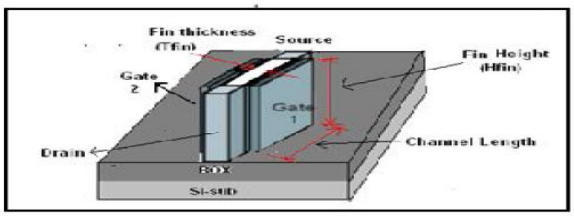

Figure (1) Cross Sectional View Of Dgfinfet

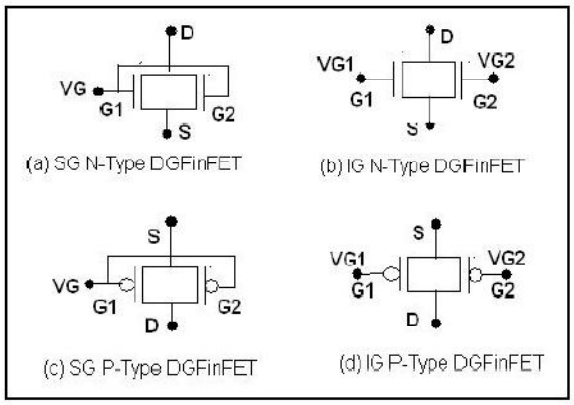

Figure (2) Different Modes Of Dgfinfet

II. PREVIOUS WORK

A lot of designs have been proposed to implement Half Adder and Half Sub-tractor with different techniques such as Pass transistors, Transmission gate, CMOS based etc. in order to reduce number of transistor counts. Half Adder and Half Sub-tractor operation perform Boolean functions on two inputs and gives two outputs.

The Half Adder circuit based on Transmission gate is described in figure3 required 12 transistors [5]. The Half sub-tractor circuit based on pass transistor in figure4 required 10 transistors [6]. Conventional CMOS Based Half adder circuit required 18 transistors and Half Sub-tractor required 20 transistors. Half Adder Boolean functions are given in equation (2) and (3).Half Sub-tractor Boolean functions are given in equation (4) and (5) -

Sum = A (XOR) B (2)
Carry = A (AND) B (3)
Difference = A (XOR) B (4)
Borrow = A' (AND) B (5)

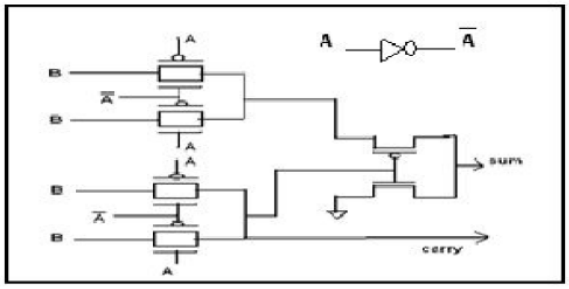

Figure (3) Design 1: 12T Half Adder Circuit

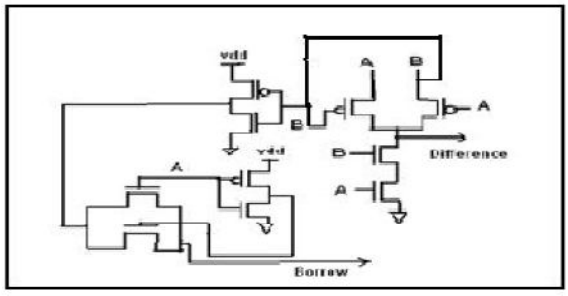

Figure (4) Design 2: 10T Half Sub-Tractor Circuit

III. PROPOSED LOGIC STRUCTURE FOR 1-BIT HALF ADDER-HALF SUB TRACTOR CELL

Addition and subtraction are basic mathematical operations performed by two different circuits inside ALU. Half Adder (fig.3) and Half Sub tractor (fig.4) circuits required total 22 transistors. The proposed design by using DGFinFET required 11 transistors (fig.8) to implement both the operations, Addition as well as sub traction. Basic Block representation of proposed design is shown in figure 5.

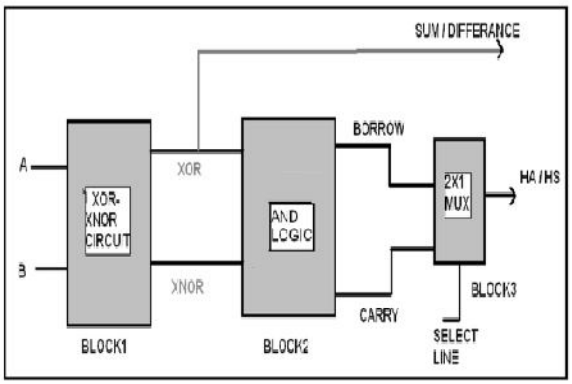

Figure (5) Block Diagram Of Proposed 1-Bit Half Adder-Half Sub Tractor Cell

Figure (5) have three basic blocks: XOR-XNOR circuit, AND logic and 2x1 multiplexer. Basic operation of proposed 1-Bit Half Adder-Half sub tractor circuit is illustrated in figure (6).

- Block 1 is two inputs and two output block. A and B are the two inputs to this block and it gives XOR and XNOR functions as outputs. As we can observe from equations (2) and (4), sum and difference inherits the property of XOR function. They can be directly derived from the XOR output of Block 1.
- In order to generate Carry and Borrow, Block 2 takes inputs from the outputs of Block 1. Carry can be generating by performing AND logic of signal B with XNOR functions. Similarly, Borrow can be generating by performing AND logic of signal B and XOR functions.
- Carry and Borrow are the outputs of Block 2, used as inputs to the Block 3. Block 3 works as 2x1 multiplexer with one select line and one output HA/HS. This select line will decide the proposed cell works as either Half Adder or Half Sub-tractor. If select line is Low then Borrow will be selected as input and transferred to the output, performed operation is Subtraction. Similarly, if select line is High then Carry will be selected as input and transferred to the output, performed operation is addition.

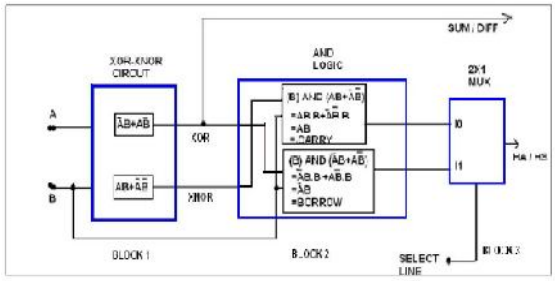

Figure (6) Basic Operation Of 1-Bit Half Adder-Half Sub Tractor Cell

Truth table representation of proposed design is shown in figure (7).

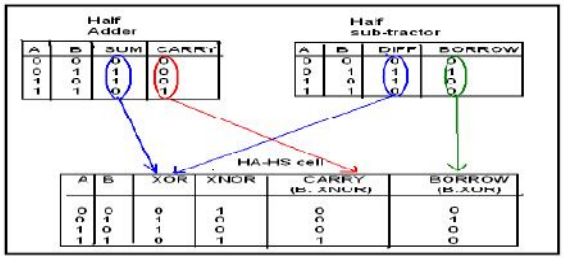

Figure (7) Truth Table Representation Of 1-Bit Half Adder-Half Sub Tractor Cell

IV. CIRCUIT REPRESENTATION AND SIMULATION OF 1-BIT HALF ADDER-HALF SUB TRACTOR CELL

Proposed design (fig.5) has been implemented with the help of DGFinFET and pass transistor concept, shown in figure (8). Let compliment of all input signals are already available.

Block (1) has 5 transistors to realize XOR and XNOR logic. Case 1: If AB=10 then transistors M1 and M3 will be ON. There will be contradiction between pull up and pull down. M1 want to give high voltage swing whereas M3 want to give low voltage swing at the XOR output node. This problem can be resolve by using proper sizing of the transistor M1.case 2: if AB=01 then M2 and M3 will be ON and M2 need to be sized to get desired XOR output voltage. The XNOR function is obtained from an inverter (M4 and M5), which has XOR as input. Case 3: if AB=00 then M1 and M2 both will be ON, XOR output will be 0 and XNOR output will be 1. Case 4: if AB=11 then M3 will be ON, XOR output will be 0 and XNOR output will be 1.

Block (2) has 4 transistors to realize Carry and Borrow functions. This block contains two AND gates: first AND Gate is forming by transistors M6 and M7, second AND Gate is forming by transistors M8 and M9. All four transistors will be either ON or OFF, depending on the state of signals B. If B is high then M6 and M8 will be ON. If B is low then M7 and M9 will be ON. XOR gives 0 for same inputs (AB=00 and AB=11) and XNOR gives 1 for same inputs. XOR gives 1 for different inputs (AB=01 and AB=10) and XNOR gives 0. Case 1: AB=00 (M7 and M9 is ON) carry and Borrow will be 0. Case 2: AB=11 (M6 and M8 is ON) carry will be 1 and Borrow will be 0. Case 3: AB=01 (M6 and M8 is ON) carry will be 0 and Borrow will be 1. Case 4: AB=10 (M7 and M9 is low) carry and Borrow both are 0.

Block (3) has 2 transistors to perform as 2X1 multiplexer. If select line is low then transistor M11 will be ON and carry will propagate to the output. If select line is high then transistor M10 will be ON and Borrow will be propagate to the output.

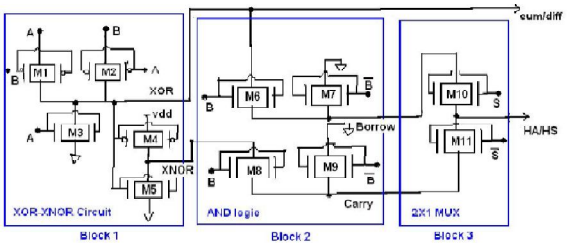

Figure (8) Circuit Representation Of 1-Bit Half Adder-Half Subtractor Cell

At voltage supply of 1.2 volt and frequency of 10MHz, simulation has been done through Cadence Specter tool. Simulated output wave for proposed design (fig. (8)) is shown in figure (9).

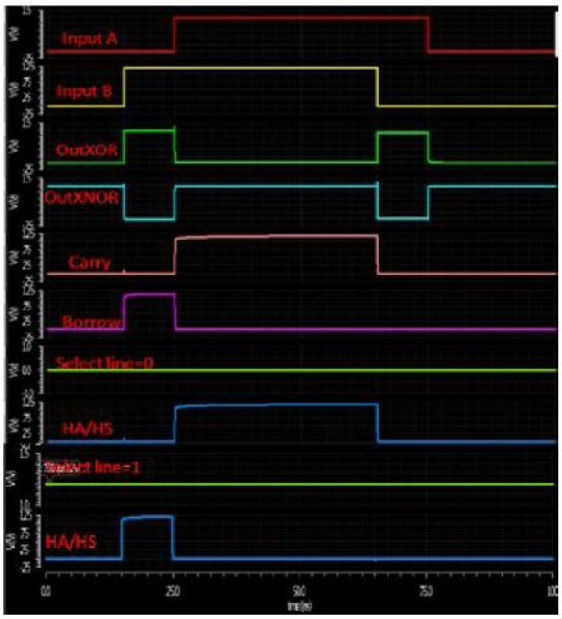

Figure (9) Simulated Output For Proposed 1-Bit Half Adder-Half Subtractor Cell

V. SIMULATION RESULTS

Design 1 (fig. 3) of Half adder circuit, is based on the Transmission gates and pass transistor. It offers the delay of 105.5 ps and Average power consumption of 10.7 uW at 180nm technology node [5]. Design 2 (fig. 4) of Half subtractor circuit, is based on pass transistors. it offers delay of 134.1 ps and Average power consumption of 12.1 uW at 180nm technology node. Output voltage levels for Design 1, Design 2 and for proposed design is illustrate in Table 1.

TABLE (1) output levels for different Designs

Input	Design1 (HA)		Design2 (FS)		Proposed Design (HA-HS) 32nm			
	Sum	Carry	Diff	Borrow	Sum	Carry	Diff	Borrow
00	Bad0	Good0	Bad0	Good0	Good0	Good0	Good0	Good0
01	Good1	Good0	Good1	Bad1	Good1	Good0	Good1	Good0
10	Good1	Good0	Good1	Good0	Good1	Good0	Good1	Good0
11	Good0	Good1	Good0	Good0	Good0	Good0	Good0	Good0

Propagation delay of the circuit gives the idea about the performance and propagation delay is the average of rise delay and fall delay.

Tpd= (Trisedelay+Tfalldelay)/2

Current from the power supply gives idea about power consumption in the circuit after multiplying this average current value with supply voltage. Average current shows how many current flows over integral with respect to time period.

TABLE (2) Different parameters for Different Designs, rise time(ps) ,fall time (ps) , rise delay (ps), fall delay (ps), Avg. current (nA), peak Current (mA)

Parameters	Design 1	Design 2	Proposd Design
Rise Time	153.7	147.6	35.1
Fall Time	134.6	145.9	28.6
Rise Delay	119.1	127.3	7.61
Fall Delay	102.3	134.5	8.23
Avg. Current	211.5	178.6	129.1
Peak Current	11.4	13.2	2.52

CONCLUSION

In this paper, the FinFET Based 1-Bit Half Adder-Half Subtractor design required less number of transistors as compares to both combine designs 1 & 2. In ALU particular arithmetic operation called by multiplexer. So, XOR-XNOR circuit and AND Logic is enough to justify the common cell operation. Block 1 & Block 2 required only 9 transistors. Number of transistor count in proposed design is approximately half compared to number of transistors in Design 1 & Design 2. The performance of the circuit has been measured by Cadence SPECTRE simulator at 32nm technology. Based on the Simulation Results, proposed design gives better output levels for all combination of input signal , better delay of 7.92 ps and better average power dissipation of 0.154 uW, compared to previous designs.

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